PHASE DIGITIZER FOR SIGNALS IN IMPERFECT QUADRATURE

The Field of the Invention

This invention relates generally to systems and methods for digitizing the phase of an analog signal. This invention relates more particularly to a system and method for continuously and accurately digitizing the phase progression of quasi-sinusoidal signals in quadrature based on digitals samples of their waveforms.

Background

Many existing phase detectors are analog in nature and have a limited dynamic range. Generally, such phase detectors generate an output voltage indicative of the phase difference between two oscillations that are close in frequency. The polarity of the output voltage indicates which oscillation is leading the other. The magnitude of the output voltage tends to be proportional to the phase difference. The dynamic range of such analog phase detectors is typically limited to one cycle in each direction. Digital phase detection is typically preferred for phase detection of dynamic ranges wider than 1 or 2 cycles.

A prior method of phase digitizing that has very wide dynamic range is described in U.S. Patent No. 5,663,666, entitled DIGITAL PHASE DETECTOR, by Chu and Sommer. Such a method can be used only on a signal operating within a very narrow frequency band, 100 ppm for example, such as a signal from a crystal oscillator. The method also requires a local oscillator operating at near coherence to the signal.

Another prior method of phase digitizing involves time-stamping the zero-crossings of a signal, as described in "Phase Digitizing Sharpens Timing Measurements," David Chu, IEEE Spectrum, July 1988, pp. 28 – 32. For precise results, such methods usually involve custom time-digitizer circuits, such as described in U.S. Patent No. 5,166,959, entitled PICOSECOND EVENT TIMER, by Chu and Knotts. Phase digitizing techniques that involve time-

stamping the zero-crossings of a signal are better suited for agile signals of high frequencies, where signal frequencies may change radically and suddenly, and many zero-crossings are available to generate time-stamp data. A penalty for such a wide-band approach is noise.

In an interferometer arrangement, noise is usually generated from fluctuating beam alignment, turbulence, photodiodes, electronic amplification, and the light source itself. In noisy environments, unexpected spurious zero-crossings may occur due to multiple triggering of the same signal edge, causing a catastrophic failure in previous phase digitizing processes.

In metrology of moving objects, signals are generally quasi-sinusoidal and of limited agility due to the physical inertia of objects being monitored. Frequency of the signal is proportional to the velocity of the object being monitored, and phase of the signal is proportional to the distance of travel. Because physical objects cannot instantaneously jump from one velocity to a much different velocity, the frequency of the signals changes relatively slowly.

The frequency of the signal, although changing slowly, may traverse a wide range, including very low frequencies where the number of zero-crossings available for measurement may be at a premium. Also, the occurrences of zero-crossings are generally non-uniform. This non-uniformity may pose additional difficulty in ascertaining the "data age" – the time between event occurrence and the presentation of its measurement data. These factors render the zero-crossing approach not an optimum technique for phase digitizing for interferometry.

A prior method of phase digitizing for interferometry uses block regression as described in U.S. Patent No. 6,480,126 entitled PHASE DIGITIZER, by Chu, and assigned to Agilent Technologies, Inc. The described method based on linear regression over an entire time segment, and not just at the vicinity of a zero crossing, is effective in averaging out noise. However, the method cannot be used on a signal operating at a frequency within ±100kHz. This frequency limit effectively places an upper limit on the velocity of the detected object when the object is moving away from the light source to avoid entering this frequency band.

Therefore, there is a need for a phase digitizing system and method that employs digital signal processing for continuously generating noise-suppressed digital phase data representing the phase of an incoming analog signal, without the disadvantages of previous phase digitizing techniques.

Summary

One aspect of the present invention provides a method of digitizing first and second signals in imperfect quadrature for obtaining characteristic parameters of the first signal. The method comprises providing a first signal, the first signal comprising an inphase quasi-sinusoidal analog signal. The method comprises providing a second signal, the second signal comprising a quadrature signal. The method comprises digitizing the first signal at a sampling rate, thereby generating a first plurality of sets of digital signal waveform samples and digitizing the second signal at the sampling rate, thereby generating a second plurality of sets of digital signal waveform samples. The method comprises digitally processing successive first and second sets of digital signal waveform samples to generate continually updated digital characteristic parameters representing a characteristic behavior of the first signal.

Brief Description of the Drawings

Figure 1 is a block diagram illustrating an exemplary embodiment of a heterodyne displacement measuring interferometer system.

Figure 2 is a diagram illustrating an exemplary embodiment of optics for generating a quadrature signal for the heterodyne displacement measuring interferometer system.

Figure 3 is an electrical block diagram illustrating an exemplary embodiment of a phase digitizer according to the present invention.

Figure 4 is an electrical block diagram illustrating the exemplary embodiment of the phase digitizer in greater detail.

Detailed Description

In the following Detailed Description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by

way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the Figure(s) being described. Because components of embodiments of the present invention can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following Detailed Description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

A displacement measuring interferometry system including phase digitizing is described in this application. Quadrature signal generation from a heterodyne source for use in the interferometry system is also described. In addition, digitized signal processing of the quadrature signal including mathematical treatment of the process and the hardware for performing the process is described. Embodiments of the invention provide a heterodyne interferometer without a low frequency limitation. The quadrature signal allows the frequency to be positive, zero, or negative without hindering phase digitizing.

I. DISPLACEMENT MEASURING INTERFEROMETRY SYSTEM

The phase digitizing system and method of the present invention is discussed in the context of a displacement measuring interferometry system. However, the phase digitizing techniques disclosed herein are also applicable to any other application in which it is desirable to continuously generate digital phase data representing the phase of an incoming analog signal.

A typical displacement measuring interferometer system consists of a frequency-stabilized laser light source, interferometer optics and measuring electronics. In metrology based on homodyne interferometry, the phase progression function $\phi(t)$ is directly proportional to the object displacement in time, t, usually by the factor $\lambda/4$. That is, one unit interval (UI) change

represents an object movement of one-quarter of the wavelength of the light wave. One UI represents one cycle of the light interference fringe, or 2π radians. In metrology based on heterodyne interferometry, there are two channels: one Doppler-shifted (Measurement Channel), and the other not shifted (Reference Channel). The difference between the two phase progression functions $\phi_M(t)$ and $\phi_R(t)$ of the two channels is proportional to the object displacement to within an arbitrary constant. The phase progression function for the reference channels is monotonically increasing with time. The phase progression function for the measurement channel increases with time only for positive frequencies, but decreases with time for negative frequencies.

Figure 1 is a block diagram illustrating a heterodyne displacement measuring interferometer system 100. Interferometer system 100 includes laser 102, interferometer 108, measurement and processing electronics 112, and quadrature generator 120. Interferometer 108 includes stationary retroreflector 104, polarizing beam splitter (PBS) 106, and movable retroreflector 110.

Laser 102 generates a pair of collinear, orthogonally polarized optical beams of equal intensity and of different frequencies *f1* and *f2*, which differ in frequency by F_R, which is a reference frequency. The optical beams pass through interferometer 108. Polarization beam splitter 106 reflects one polarization of the incoming light to stationary retroreflector 104, and passes the other polarization of light to movable retroreflector 110. Retroreflectors 104 and 110 return the light to polarization beam splitter 106, where one beam is transmitted and the other beam is reflected, so that the two beams are again collinear and cobore. Linear motion of movable retroreflector 110 results in a corresponding change in the difference in phase between the two beams. The output beams from interferometer 108 are optically processed in quadrature generator 120 to produce two mixed beams 113 F_M (Inphase) and 114 Q_M (quadrature), both fluctuating in intensity coherently but out of phase. The frequency of fluctuation is in accordance with Doppler shifting of the split-frequency. Both beams are photo-detected and processed in measurement and processing electronics 112. A third reference fluctuating beam F_R 111, not Doppler shifted, is phase digitized by a processor similar to one described in

U.S. Patent No. 6,480,126. Either mixed beam is referred to as the measurement signal, and the mixing is represented by the following Equation I:

Equation I

Measurement signal = $\underline{f1} \otimes f2$

where:

$\otimes$ indicates a mixing operation; and

the underlining of $f1$ indicates that the signal is Doppler-shifted.

Measurement and processing electronics 112 contain a photodetector that produces an electrical measurement signals corresponding to the optical measurement signals. The measurement signal has a frequency that is equal to the reference frequency F_R plus the Doppler shift frequency:

Equation II

$$F_M = F_R + nv/\lambda$$

where:

v is the velocity of the interferometer element whose position is being measured (the sign of v indicates the direction of travel);

λ is the wavelength of light emitted from laser 102; and

n equals 2, 4, etc., depending on the number of passes the light makes through interferometer 108.

In the example system of Figure 1, the movement of retroreflector 110 produces the Doppler shift and n is equal to 2. The reference signal is produced by mixing the two beams from laser 102 ($f1$ and $f2$), which is represented by the following Equation III:

Equation III

Reference Signal = $f1 \otimes f2$

Measurement and processing electronics 112 contain a photodetector that produces an electrical reference signal corresponding to the optical reference signal. The reference signal has a frequency that is equal to the reference frequency F_R.

Measurement and processing electronics 112 measure the phase difference between the reference signal and the measurement signal, and process the difference to provide position and velocity outputs.

Previous methods for determining and processing phase information employ analog techniques or digital techniques that involved time-stamping the zero-crossings of the signal, or techniques that are of limited frequency range. Embodiments of the present invention provide a more effective technique for generating digitized phase information for interferometry applications such as that shown in Figure 1, as well as any other application where it is desirable to generate digital phase data representing the instantaneous phase of an incoming analog signal.

One embodiment of the present invention is a method of continuously and accurately digitizing the phase progression of a quasi-sinusoidal signal based on digital samples of its waveform. When the signal comes from a Doppler-shifted light wave reflected from a moving object, possibly down-converted by an interferometer, the signal phase is directly proportional to the position of the object. Therefore, continuous signal phase monitoring is equivalent to continuous position monitoring of the object, accurate to a fraction of the light wavelength.

Phase digitizing of an analog quasi-sinusoidal signal with a low frequency limit of ±100 kHz is described in U.S. Patent No. 6,480,126, entitled PHASE DIGITIZER, issued November 12, 2002 to Chu and assigned to Agilent Technologies, Inc., and is incorporated herein by reference. To overcome the low frequency limitation, a quadrature, or substantially quadrature signal is generated from light exiting interferometer 108.

In one aspect of the invention, a quasi-sinusoidal inphase signal of unknown and changing frequency, phase, and magnitude is digitized by a first analog-to-digital converter (ADC) at a regular rate greater than twice the bandwidth of the signal. At the same time, a quadrature signal for the inphase signal is digitized by a second ADC at the same rate as the inphase signal. The digitized data from both the inphase and quadrature signals is analyzed in 256-sample segments. For each 256-sample segment, a "best-fit" estimate of the inphase signal is generated of the form $V*\cos[2\pi(Freq*i-\theta)]$, and a "best-fit" estimate of the quadrature signal is generated of the form $U*\sin[2\pi(Freq*i-\theta+\Delta\theta)]$, where i is an index for identifying consecutive digital signal samples

within a segment, V and U represent magnitude estimates of the inphase and quadrature signals respectively, *Freq* represents a frequency estimate, θ represents a phase-offset estimate, and $\Delta\theta$ represents a phase error estimate.

II. QUADRATURE SIGNAL GENERATION FROM A HETERODYNE SOURCE

For quadrature detection of the measurement signal, a second, additional heterodyned signal is generated from the light exiting interferometer 108. The second signal has a phase shift of 90 degrees from the first heterodyned signal. The 90 degree phase shift between heterodyned signals is accomplished by inducing a 90 degree phase shift between the *f1* and *f2* frequency components in the second beam. This signal is then treated exactly as the first mixed heterodyned signal. The beam is sent through a polarizer and the mixed heterodyned signal is sent to a second detector.

Figure 2 is a diagram illustrating the preferred embodiment of quadrature Generator 120. The optics in quadrature generator 120 includes a non-polarizing beam splitter 132, quarter wave plate 136, and two polarizers 140 and 146.

The process for developing the two heterodyned signals is as follows. First, the beam exiting interferometer 108, indicated at 130, is split spatially into two beams, 134 and 144, each with approximately equal amounts of *f1* and *f2* frequency components using non-polarizing beam splitter 132. The *f1* and *f2* frequency components in beams 134 and 144 remain orthogonally polarized. In one embodiment, non-polarizing beam splitter 132 is a 50% non-polarizing beam splitter or other suitable non-polarizing beam splitter.

Second, quarter wave plate 136 is inserted in the path of beam 134 such that its fast axis is located at 45 degrees to the orthogonally polarized *f1* and *f2* frequency components in beam 134. Quarter wave plate 136 changes the orthogonally linearly polarized light beam 134 to orthogonally circularly polarized light beam 138, which is right and left circularly polarized light.

The preceding two steps have produced two beams, 138 and 144 from beam 130 exiting interferometer 108. In beam 144, the *f1* and *f2* frequency

components are in orthogonal and linear polarization states. In beam 138, the *f1* and *f2* frequency components are in orthogonal and circular polarization states.

Third, both beams 138 and 144 pass through polarizers. Beam 138 passes through polarizer 140 and beam 144 passes through polarizer 146. The polarizer axis of polarizer 146 is oriented at 45 degrees to the orthogonally polarized *f1* and *f2* frequency components of linearly polarized beam 144.

Mathematical treatment of the signal mixing for beam 144 is as follows. The nomenclature $\mathbf{E}_1$ and $\mathbf{E}_2$ is assigned to the two linearly polarized components of optical frequencies *f1* and *f2* respectively. For simplicity, the electric fields of the polarized beams are written in column vectors (Jones Vectors) as follows:

Equation IV

$$\mathbf{E}_1 = \begin{bmatrix} Ae^{i(2\pi f_1 t+\delta_1)} \\ 0 \end{bmatrix}$$

Equation V

$$\mathbf{E}_2 = \begin{bmatrix} 0 \\ Ae^{i(2\pi f_2 t+\delta_2)} \end{bmatrix}$$

These signals are projected onto polarizer 146 with its polarizer axis oriented at 45 degrees to the orthogonally polarized *f1* and *f2* frequency components of linearly polarized beam 144.

The Jones Matrix for a polarizer with its polarizer axis oriented at 45 degrees is:

Equation VI

$$\mathbf{P}_{45} = \left(\frac{1}{2}\right) * \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$$

$\mathbf{E}_1$ and $\mathbf{E}_2$ pass through polarizer 146 and become $\mathbf{E}_{1out}$ and $\mathbf{E}_{2out}$, where:

Equation VII

$$\mathbf{E}_{1out} = \left(\frac{1}{2}\right) * \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} * \begin{bmatrix} Ae^{i(2\pi f_1 t+\delta_1)} \\ 0 \end{bmatrix} = \left(\frac{1}{2}\right) * \begin{bmatrix} Ae^{i(2\pi f_1 t+\delta_1)} \\ Ae^{i(2\pi f_1 t+\delta_1)} \end{bmatrix}$$

Equation VIII

$$\mathbf{E}_{2out} = \left(\frac{1}{2}\right) * \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} * \begin{bmatrix} Ae^{i(2\pi f_2 t + \delta_2)} \\ 0 \end{bmatrix} = \left(\frac{1}{2}\right) * \begin{bmatrix} Ae^{i(2\pi f_2 t + \delta_2)} \\ Ae^{i(2\pi f_2 t + \delta_2)} \end{bmatrix}$$

The sum of $\mathbf{E}_{1out}$ and $\mathbf{E}_{2out}$ exiting polarizer 146 equals signal 148 as follows:

Equation IX

$$\mathbf{E}_{1out} + \mathbf{E}_{2out} = \left(\frac{1}{2}\right) * \begin{bmatrix} Ae^{i(2\pi f_1 t + \delta_1)} + Ae^{i(2\pi f_2 t + \delta_2)} \\ Ae^{i(2\pi f_1 t + \delta_1)} + Ae^{i(2\pi f_2 t + \delta_2)} \end{bmatrix}$$

For circularly polarized beam 138, the amount of phase difference between the *f1* and *f2* frequency components can be varied by the rotational orientation of the polarizer axis of polarizer 140. If the axis of polarizer 140 is aligned with the fast axis of quarter wave plate 136, there is no phase difference between the *f1* and *f2* frequency components. If the polarizer axis of polarizer 140 is oriented at 45 degrees to the fast axis of quarter wave plate 136, the phase difference is 90 degrees. The general rule is that for every degree of rotation of the polarizer axis of polarizer 140 off from alignment to the fast axis of quarter wave plate 136, the phase difference will increase (or decrease) by two degrees.

Mathematical treatment of the signal mixing for beam 134 is as follows. The nomenclature $\mathbf{E}_3$ and $\mathbf{E}_4$ is assigned to the two linearly polarized components of optical frequencies *f1* and *f2* respectively. Beam 134 is changed into circularly polarized components of optical frequencies *f1* and *f2* respectively as follows:

Equation X

$$\mathbf{E}_3 = \begin{bmatrix} Ae^{i(2\pi f_1 t + \delta_1)} \\ 0 \end{bmatrix}$$

Equation XI

$$\mathbf{E}_4 = \begin{bmatrix} 0 \\ Ae^{i(2\pi f_2 + \delta_2)} \end{bmatrix}$$

The Jones Matrix for quarter wave plate 136 with its fast axis set at 45 degrees is:

Equation XII

$$\mathbf{Q}_{45} = \left(\frac{1}{\sqrt{2}}\right)\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}$$

The Jones Matrix for polarizer 140 with its polarizer axis set at 90 degrees is:

Equation XIII

$$\mathbf{P}_{90} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}$$

By multiplying equations X, XII, and XIII and equations XI, XII, and XIII, through transformation $\mathbf{E}_3$ and $\mathbf{E}_4$ become $\mathbf{E}_{3out}$ and $\mathbf{E}_{4out}$ as follows.

For $\mathbf{E}_{3out}$:

Equation XIV

$$\mathbf{E}_{3out} = \left(\frac{1}{\sqrt{2}}\right) * \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix} * \begin{bmatrix} Ae^{i(2\pi f_1 t + \delta_1)} \\ 0 \end{bmatrix}$$

Equation XIV reduces to:

Equation XV

$$\mathbf{E}_{3out} = \left(\frac{1}{\sqrt{2}}\right) * \begin{bmatrix} 0 \\ Ae^{i(2\pi f_1 t + \delta_1 + \pi/2)} \end{bmatrix}$$

For $\mathbf{E}_{4out}$:

Equation XVI

$$\mathbf{E}_{4out} = \left(\frac{1}{\sqrt{2}}\right) * \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix} * \begin{bmatrix} 0 \\ Ae^{i(2\pi f_2 t + \delta_2)} \end{bmatrix}$$

Equation XVI reduces to:

Equation XVII

$$\mathbf{E}_{4out} = \left(\frac{1}{\sqrt{2}}\right) * \begin{bmatrix} 0 \\ Ae^{i(2\pi f_2 t + \delta_2)} \end{bmatrix}$$

The sum of $\mathbf{E}_{3out}$ and $\mathbf{E}_{4out}$ exiting polarizer 140 equals signal 142 as follows:

Equation XVIII

$$\mathbf{E}_{3out} + \mathbf{E}_{4out} = \left(\frac{1}{\sqrt{2}}\right) * \begin{bmatrix} 0 \\ Ae^{i(2\pi f_1 t + \delta_1 + \pi/2)} + Ae^{i(2\pi f_2 t + \delta_2)} \end{bmatrix}$$

Equations IV-IX show that the heterodyne signal generated from combining $\mathbf{E}_{1out}$ and $\mathbf{E}_{2out}$ does not add additional phase to the mixed signal, but that combining $\mathbf{E}_{3out}$ and $\mathbf{E}_{4out}$ through equations X-XVIII does add a 90 degree phase shift between the *f1* and *f2* frequency components.

Signals 142 and 148 are in imperfect quadrature. Signal 148 is referred to as the inphase signal and signal 142 is referred to as the quadrature signal. Quadrature signal 142 has a phase shift of 90 degrees to inphase signal 148.

III. DIGITIZED SIGNAL PROCESSING

Figure 3 is a block diagram illustrating an exemplary embodiment of phase digitizer 200. Phase digitizer 200 digitally processes incoming inphase signal *V* 148 and quadrature signal *U* 142. Phase digitizer 200 includes analog-to-digital converters (ADCs) 212 and 214, digital signal processor 202, and phase accumulator 208. Phase digitizer 200 uses a block regression technique for phase digitizing in the steady state.

Inphase signal *V* 148 is input to ADC 212 and quadrature signal *U* 142 is input to ADC 214. ADC 212 is electrically coupled to digital signal processor 202 through data path 213 and ADC 214 is electrically coupled to digital signal processor 202 through data path 215. Phase accumulator 208 is electrically coupled to digital signal processor 202 through path 209. Digital signal processor 202 is electrically coupled to phase-accumulator 208 through path 203

comprising frequency update *Freq* 220 and phase correction θ_{cor} 218. Continuous phase output signal *Phi(j)* 216 is provided by digital signal processor 202, latched at mid-segment by latch 258.

Inphase signal *V* 148 and quadrature signal *U* 142 in imperfect quadrature are processed using digital signal processing by phase digitizer 200. ADC 212 samples inphase signal *V* 148 and ADC 214 samples quadrature signal *U* 142 and provides the output samples continuously to digital signal processor 202. In one embodiment, ADCs 212 and 214 are 12-bit ADCs and sample inphase signal *V* 148 and quadrature signal *U* 142 at 80 MHz. In other embodiments, other suitable sampling rates can be used. In this embodiment, the samples are labeled as vectors **V**, for inphase signal *V* 148, and **U**, for quadrature signal *U* 142, each of length 256. Each segment is therefore 256/80MHz or 3.2 μs.

Phase accumulator 208 approximates the signal phase progression $\phi(t_i)$ of incoming inphase signal *V* 148, where the index "*i*" indicates an 80-MHz clock count value. Successive t_i's are separated by τ, the period of 80 MHz.

Phase digitizer 200 accurately digitizes the phase progression (in unit intervals UI) of inphase signal *V* 148 at the 3.2 μs rate regardless of the inphase signal *V* 148 frequency. The inphase signal *V* 148 frequency can be positive, negative, near or at zero, or anywhere within the overall measurement range of approximately ± 40 MHz.

When the inphase signal *V* 148 frequency is above approximately +300 kHz or below -300 kHz (referred to as normal frequency range), one vector, **V**, is used for phase digitizing (as described in U.S. Patent No. 6,480,126) by digital signal processor 202. Under this normal frequency range, imperfections of **U** are measured and calibrated by digital signal processor 202. Imperfections, including the magnitude ratio $r = |V/U|$ and phase error $\Delta\theta$ (departure from 90° of quadrature signal *U* 142 to inphase signal *V* 148), are relatively constant. These parameters can be exported by digital signal processor 202 and used later in near-zero or at-zero frequency range to minimize errors.

When the inphase signal *V* 148 frequency is between approximately –300 kHz and +300 kHz (referred to as low frequency range), including zero

frequency, both vectors **U** and **V** are used for phase digitizing by digital signal processor 202. However, by using calibration data of r and $\Delta\theta$, exported from previous measurements under normal frequencies, the effect due to imperfections of **U** are corrected.

The following is the mathematical formulation for phase digitizer 200, including digital signal processor 202. The mathematical model for inphase signal V 148 and quadrature signal U 142 at the 12.5 ns rate (one 80 MHz cycle) is:

Equation XIX

$$V_i = V\cos 2\pi(ft_i - \theta) + noise$$

Equation XX

$$U_i = U\sin 2\pi(ft_i - \theta + \Delta\theta) + noise$$

Inphase signal V 148 and quadrature signal U 142 are in imperfect quadrature because $U \neq V$ and $\Delta\theta \neq 0$. After expansion of cosine and sine equations XIX and XX become:

Equation XXI

$$V_i = X_V \cos 2\pi ft_i + Y_V \sin 2\pi ft_i + noise$$

Equation XXII

$$U_i = X_U \sin 2\pi ft_i + Y_U \cos 2\pi ft_i + noise$$

Two 256-length operation vectors **E** and **D** are defined, where:

Equation XXIII

E = (e,e,e,...e)

where e=1 if $0.25 \leq ft_i < 0.50$; e = −1 if $0.75 \leq ft_i < 1.0$; else e = 0.

Equation XXIV

D = (d,d,d,...,d)

where d=1 if $0 \leq ft_i < 0.25$; d = − 1 if $0.50 \leq ft_i < 0.75$; else d = 0.

Four 256-length data vectors **V**, **U**, **C**, and **S** are defined, where:

Equation XXV

$\mathbf{V}= (V_1,V_2,\ldots,V_{256})$, containing the 256 samples of V.

Equation XXVI

$\mathbf{U} = (U_1,U_2,\ldots,U_{256})$, containing the 256 samples of U.

Equation XXVII

$\mathbf{C} = (\cos ft_1, \cos ft_2,\ldots, \cos ft_{256})$, containing cosine table values addressed by ft_i.

Equation XXVIII

$\mathbf{S} = (\sin ft_1, \sin ft_2,\ldots, \sin ft_{256})$ containing sine table values addressed by ft_i.

At normal frequencies (i.e. outside ± 300 kHz), the 512 equations can be reduced to four equations by **E** and **D** operating on **V**, **U**, **C**, and **S**:

Equation XXIX

$$(\mathbf{D}\cdot\mathbf{V}) = X_V(\mathbf{D}\cdot\mathbf{C}) + Y_V(\mathbf{D}\cdot\mathbf{S})$$

Equation XXX

$$(\mathbf{E}\cdot\mathbf{V}) = X_V(\mathbf{E}\cdot\mathbf{C}) + Y_V(\mathbf{E}\cdot\mathbf{S})$$

Equation XXXI

$$(\mathbf{D}\cdot\mathbf{U}) = X_U(\mathbf{D}\cdot\mathbf{S}) - Y_U(\mathbf{D}\cdot\mathbf{C})$$

Equation XXXII

$$(\mathbf{E}\cdot\mathbf{U}) = X_U(\mathbf{E}\cdot\mathbf{S}) - Y_U(\mathbf{E}\cdot\mathbf{C})$$

At normal frequencies, computation of V, θ, r = $|V/U|$, and $\Delta\theta$ is based on 512 equations and four unknowns X_V, Y_V, X_U and Y_U. Equations XXIX and XXX and equations XXXI and XXXII are both independent sets and can be used to solve separately for unknowns X_V, Y_V and X_U, Y_U respectively as follows:

Equation XXXIII

$$\begin{bmatrix} X_V \\ Y_V \end{bmatrix} = \begin{bmatrix} (\mathbf{E}\cdot\mathbf{S}) & -(\mathbf{D}\cdot\mathbf{S}) \\ -(\mathbf{E}\cdot\mathbf{C}) & (\mathbf{D}\cdot\mathbf{C}) \end{bmatrix} \cdot \begin{bmatrix} (\mathbf{D}\cdot\mathbf{V}) \\ (\mathbf{E}\cdot\mathbf{V}) \end{bmatrix}$$

Equation XXXIV

$$\begin{bmatrix} X_U \\ Y_U \end{bmatrix} = \begin{bmatrix} -(\mathbf{E}\cdot\mathbf{C}) & (\mathbf{D}\cdot\mathbf{C}) \\ -(\mathbf{E}\cdot\mathbf{S}) & (\mathbf{D}\cdot\mathbf{S}) \end{bmatrix} \cdot \begin{bmatrix} (\mathbf{D}\cdot\mathbf{U}) \\ (\mathbf{E}\cdot\mathbf{U}) \end{bmatrix}$$

Using a four-quadrant actangent function, the parameter θ_{cor} (in UI) for tracking and phase digitizing signal V is computed as follows:

Equation XXXV

$$\theta_{cor} = \left(\frac{1}{2\pi}\right)\arctan(X_V, Y_V)$$

The calibration parameters r and $\Delta\theta$ (in UI) are computed as follows:

Equation XXXVI

$$\mathrm{r} = \left|\frac{V}{U}\right| = \sqrt{\frac{X_V^2 + Y_V^2}{X_U^2 + Y_U^2}}$$

Equation XXXVII

$$\Delta\theta = \left(\frac{1}{2\pi}\right) Arc\tan\left(\frac{X_U Y_V - X_V Y_U}{X_V X_U + Y_V Y_U}\right)$$

The calibration parameters r and $\Delta\theta$ are averaged over several segments of 3.2 μs and exported. They are used when the signal frequency becomes low, (i.e. within ±300 kHz). To generate these parameters, the usual determinant for the inversion need not be explicitly computed.

At low frequencies (i.e. within ± 300 kHz), equations XXIX-XXXII may not be linearly independent. Both V and U cannot be computed separately with confidence. By using calibration factors r and $\Delta\theta$, however, the necessary V and θ_{cor} can be accurately computed. The calibration factor r remains relatively constant even as V and U fluctuate. To equalize the magnitudes, the last two equations (Equations XXXI and XXXII) are multiplied by the calibration factor r exported. To account for the non-ideal skew of the two signals, $\Delta\theta$ is added to the address of the sine and cosine tables by U. These two steps effectively

change (X_u, Y_u) to (X_v, Y_v) and create four sums $(\mathbf{D}\cdot\mathbf{S})_U$, $(\mathbf{D}\cdot\mathbf{C})_U$, $(\mathbf{E}\cdot\mathbf{S})_U$, $(\mathbf{E}\cdot\mathbf{C})_U$. Thus modified, equations XXXI and XXXII become:

Equation XXXVIII

$$r(\mathbf{D}\cdot\mathbf{U}) = X_V(\mathbf{D}\cdot\mathbf{S})_u - Y_V(\mathbf{D}\cdot\mathbf{C})_u$$

Equation XXXIX

$$r(\mathbf{E}\cdot\mathbf{U}) = X_V(\mathbf{E}\cdot\mathbf{S})_u - Y_V(\mathbf{E}\cdot\mathbf{C})_u$$

There are two unknowns X_V and Y_V in equations XXIX, XXX, XXXVIII, and XXXIX. The four equations are combined to form two equations XL and XLI as follows for maximum independence:

Equation XL

$$(\mathbf{D}\cdot\mathbf{V}) + r\cdot(\mathbf{E}\cdot\mathbf{U}) = X_V[(\mathbf{D}\cdot\mathbf{C}) + (\mathbf{E}\cdot\mathbf{S})_u] + Y_V[(\mathbf{D}\cdot\mathbf{S}) - (\mathbf{E}\cdot\mathbf{C})_u]$$

Equation XLI

$$(\mathbf{E}\cdot\mathbf{V}) - r\cdot(\mathbf{D}\cdot\mathbf{U}) = X_V[(\mathbf{E}\cdot\mathbf{C}) - (\mathbf{D}\cdot\mathbf{S})_u] + Y_V[(\mathbf{E}\cdot\mathbf{S}) + (\mathbf{D}\cdot\mathbf{C})_u]$$

The solution to this 2-by-2-equation set in matrix notation is:

Equation XLII

$$\begin{bmatrix} X_V \\ Y_V \end{bmatrix} = \begin{bmatrix} (\mathbf{E}\cdot\mathbf{S}) + (\mathbf{D}\cdot\mathbf{C})_u & (\mathbf{E}\cdot\mathbf{C})_u - (\mathbf{D}\cdot\mathbf{S}) \\ (\mathbf{D}\cdot\mathbf{S})_u - (\mathbf{E}\cdot\mathbf{C}) & (\mathbf{D}\cdot\mathbf{C}) + (\mathbf{E}\cdot\mathbf{S})_u \end{bmatrix} \cdot \begin{bmatrix} (\mathbf{D}\cdot\mathbf{V}) + r\cdot(\mathbf{E}\cdot\mathbf{U}) \\ (\mathbf{E}\cdot\mathbf{V}) - r\cdot(\mathbf{D}\cdot\mathbf{U}) \end{bmatrix}$$

Finally, using a four-quadrant arctangent function, the low-frequency phase-digitizing parameter θ_{cor} (in UI) is:

Equation XLIII

$$\theta_{cor} = \frac{1}{2\pi}\arctan(X_V, Y_V)$$

Figure 4 illustrates phase digitizer 200, including digital signal processor 202 illustrated in Figure 3 in greater detail. Digital signal processor 202 includes arithmetic logic units (ALUs) 204a-204l (collectively referred to as ALUs 204), adder 260, cosine table U 228, cosine table V 230, sine table U 232, sine table V 234, inverters 220 and 222, digital processing block 210, counter 254, latch 258, inverter 252, and registers 256.

ADC 212 is electrically coupled to ALU **E·V** 204a and ALU **D·V** 204b. ADC 214 is electrically coupled to ALU **D·U** 204g and ALU **E·U** 204h. Cosine table U 228 is electrically coupled to ALU $\mathbf{D \cdot C_U}$ 204i and ALU $\mathbf{E \cdot C_U}$ 204j. Cosine table V 230 is electrically coupled to ALU **E·C** 204c and ALU **D·C** 204d. Sine table U 232 is electrically coupled to ALU $\mathbf{D \cdot S_U}$ 204k and ALU $\mathbf{E \cdot S_U}$ 204l. Sine table V 234 is electrically coupled to ALU **E·S** 204e and ALU **D·S** 204f.

The outputs of ALUs 204 are electrically coupled to registers 256. The output of adder 260 is electrically coupled to cosine table U 228 and sine table U 232. The inputs of adder 260 are electrically coupled to digital processing block 210 through path 219 and the output of phase accumulator 210 through path 209. The output of phase accumulator 208 is electrically coupled to cosine table V 230 and sine table V 234 through path 209. The output of phase accumulator 208 is electrically coupled to the polarity (SGN) inputs of ALUs 204 through path 209 and inverter 220. The output of phase accumulator 208 is electrically coupled to and the clock enable (CE) inputs of ALUs 204a, 204c, 204e, 204h, 204j, and 204l through path 209 and the CE inputs of ALUs 204b, 204d, 204f, 204g, 204i, and 204k through path 209 and inverter 222. The output of phase accumulator 208 is electrically coupled to *Phi(j)* latch 258 through high speed phase output path 209.

Phi(j) latch 258 is electrically coupled to digital processing block 210 through path 259. Registers 256 are electrically coupled to digital processing block 210 through path 257. Clock signal 252 is input to modulo-2^8 counter 254. Modulo-2^8 counter 254 is electrically coupled to *Phi(j)* latch 258 through inverter 252 and to registers 256 through path 255.

The twelve dot products used in equations XXIX through XLIII, **(D·V)**, **(D·U)**, **(D·C)**, **(D·S)**, **(E·V)**, **(E·U)**, **(E·C)**, **(E·S)**, $\mathbf{(D \cdot C)_U}$, $\mathbf{(D \cdot S)_U}$, $\mathbf{(E \cdot C)_U}$, $\mathbf{(E \cdot S)_U}$, are synthesized by hardware at high speed by ALUs 204 by the same names.

In one embodiment, the digital circuits shown in Figure 4 are clocked synchronously at an 80 MHz rate. The clocking circuit is omitted from Figure 4 to simplify the illustration of the invention.

ADCs 212 and 214 are 12-bit ADCs that digitize at 80 MHz the incoming inphase signal 148 from photodetector 270 of unknown magnitude, frequency, and phase and incoming quadrature signal 142 from photodetector 272, respectively. In alternative embodiments, other sampling rates can be used. The output of ADC 212 is monitored simultaneously by two ALUs 204a and 204b. The output of ADC 212 is represented by **V** from equation XXV. The output of ADC 214 is monitored simultaneously by two ALUs 204g and 204h. The output of ADC 214 is represented by **U** from equation XXVI.

In one embodiment, phase accumulator 208 is a 42-bit phase accumulator and approximates the signal phase progression $\phi(t_i)$ of incoming inphase signal 148, where the index "i" indicates a clock count value. Successive t_i's are separated by τ, the period of 80 MHz. The most significant 25 bits of phase accumulator 208 represent the numbers of whole UI in $\phi(t_i)$, and the remaining 17 bits represent fractional UI in $\phi(t_i)$. The increment value of phase accumulator 208, *Freq*, indicated at 220, is the latest estimate of the signal frequency expressed in UI/τ.

In one embodiment, the most significant 8 bits of the fractional output of phase accumulator 208 are used to address cosine table V 230 and sine table V 234. Tables 230 and 234 each span one complete period in the 8-bit address space. Therefore, there are 256 entries that span one period in each table 230 and 234. In one embodiment, each entry in tables 230 and 234 is 10 bits wide. The output of cosine table V 230 is presented to ALU 204c and ALU 204d. The output of cosine table V 230 is represented by **C** from equation XXVII. The output of sine table V 234 is presented to ALU 204e and ALU 204f. The output of sine table V 234 is represented by **S** from equation XXVIII.

The most significant 8 bits of the fractional output of phase accumulator 208 are modified by $\Delta\theta$ in adder 260 to create the dot products with U-suffixes. The output of adder 260 is used to address cosine table U 228 and sine table U 232. Tables 228 and 232 each span one complete period in the 8-bit address space. Therefore, there are 256 entries that span one period in each table 228 and 232. Each entry in tables 228 and 232 is 10 bits wide. The output of cosine table U 228 is presented to ALU 204i and ALU 204j. The output of sine table U

232 is presented to ALU 204k and ALU 204l. The output of cosine table U 228 and sine table U 232 is first used in equation XXXVIII.

The two most significant bits of the fractional part of the output of phase accumulator 208 determine the quadrants and control the operations of the twelve ALUs 204. The two most significant bits enable or disable the twelve ALUs 204 and assign the polarity of accumulation for the enabled units as shown in the following Table I:

Table I

bits	Name	Action
00	1st quadrant	ALUs 204b, 204d, 204f, 204g, 204i, and 204k are enabled to increment, ALUs 204a, 204c, 204e, 204h, 204j, and 204l are disabled
01	2nd quadrant	ALUs 204a, 204c, 204e, 204h, 204j, and 204l are enabled to increment, ALUs 204b, 204d, 204f, 204g, 204i, and 204k are disabled
10	3rd quadrant	ALUs 204b, 204d, 204f, 204g, 204i, and 204k are enabled to decrement, ALUs 204a, 204c, 204e, 204h, 204j, and 204l are disabled
11	4th quadrant	ALUs 204a, 204c, 204e, 204h, 204j, and 204l are enabled to decrement, ALUs 204b, 204d, 204f, 204g, 204i, and 204k are disabled

The operation of Table I is represented by the operational vectors **E** and **D**, defined in equations XXIII and XXIV. The CE inputs of ALUs 204 are enabled when there is a need to add or to subtract and the CE inputs of ALUs 204 are disabled when **E** or **D** should do nothing (i.e. when $e = 0$ or $d = 0$).

In one embodiment, the digitized data from ADCs 212 and 214 is analyzed in 256-sample segments. Modulo-2^8 counter 254 sequences the events in each 256-clock segment. At the negative transition of counter 254, halfway into a segment, 16 bits of output of phase accumulator 208 (6 bits of whole UI and 10 bits of fractional UI) are latched by *Phi(j)* latch 258. The latched value represents

a temporary mid-segment value, *Phi(j)*, which is held in reserve to be modified at the end of the segment. The letter "*j*" is an index for identifying segments.

At the positive transition of counter 254 at the end of a segment, the outputs of the twelve ALUs 204 are latched into twelve registers 256, omitting the 4 least significant bits. The latched values are **E·V**, **D·V**, **E·C**, **D·C**, **E·S**, **D·S**, **D·U**, **E·U**, $\mathbf{D \cdot C_U}$, $\mathbf{E \cdot C_U}$, $\mathbf{D \cdot S_U}$, and $\mathbf{E \cdot S_U}$, which are associated with ALUs 204a, 204b, 204c, 204d, 204e, 204f, 204g, 204h, 204i, 204j, 204k, and 204l, respectively. Immediately after the values are latched, all twelve ALUs 204 are reset to zero (reset circuit not shown for clarity purposes) so that ALUs 204 are ready for the next segment.

The latched values of the twelve ALUs 204 are digitally processed by digital processing block 210 as shown in the following Equations XLIV through LVIII:

The temporary mid-segment value *Phi(j)* latched by *Phi(j)* latch 258 is now corrected by a computed parameter θ_{cor} as follows:

Equation XLIV

$$Phi(j) = Phi(j) - \theta_{cor}$$

Simultaneously, the current value ~~of~~ ϕ of the phase accumulator 208 is also corrected by computed parameter θ_{cor} as follows:

Equation XLV

$$\phi = \phi - \theta_{cor}$$

The corrected *Phi(j)*, together with 320 values from past segments, are stored in memory and exported as measured phase progression values. An updated frequency value, *Freq*, under steady state, is derived from the current value *Phi(j)* and one historical value *Phi(j–1)* recorded one segment ago. One embodiment of the formulation for the new steady-state *Freq* is:

Equation XLVI

$$Freq = [Phi(j) - Phi(j-1)]/256$$

Exporting *Phi(j)* completes the tracking and phase digitizing process, which is the same for all frequencies, including normal, low, positive, zero or negative frequency. However, how computed parameter θ_{cor} is computed depends on the signal frequency.

As previously described, there are two basic modes of operation, including operation at normal frequencies and operation at low frequencies. No special consideration is necessary to handle positive and negative frequencies. The generation of dot products by ALUs 204 and phase tracking and correction by computed parameter θ_{cor} are the same for either mode. The following equations XLVII through LVIII show how the dot products from ALUs 204 are used to generate the phase correction computed parameter θ_{cor} in each mode during digital processing in digital processing block 210.

Normal frequencies: outside ±300 kHz (i.e. *Freq* outside ±0.00375)

In this mode, four dot products $\mathbf{D}\cdot\mathbf{C}_U$ from ALU 204i, $\mathbf{D}\cdot\mathbf{S}_U$ from ALU 204k, $\mathbf{E}\cdot\mathbf{C}_U$ from ALU 204j, and $\mathbf{E}\cdot\mathbf{S}_U$ from ALU 204l are not used.

Four intermediate parameters *Xv*, *Yv*, *Xu*, *Yu* are derived from the remaining eight dot products as follows:

Equation XLVII

$$X_V = (\mathbf{E}\cdot\mathbf{S})(\mathbf{D}\cdot\mathbf{V}) - (\mathbf{D}\cdot\mathbf{S})(\mathbf{E}\cdot\mathbf{V})$$

Equation XLVIII

$$Y_V = (\mathbf{D}\cdot\mathbf{C})(\mathbf{E}\cdot\mathbf{V}) - (\mathbf{E}\cdot\mathbf{C})(\mathbf{D}\cdot\mathbf{V})$$

Equation XLIX

$$X_U = (\mathbf{D}\cdot\mathbf{C})(\mathbf{D}\cdot\mathbf{U}) - (\mathbf{E}\cdot\mathbf{C})(\mathbf{E}\cdot\mathbf{U})$$

Equation L

$$Y_U = (\mathbf{D}\cdot\mathbf{S})(\mathbf{E}\cdot\mathbf{U}) - (\mathbf{E}\cdot\mathbf{S})(\mathbf{D}\cdot\mathbf{U})$$

The two quadrature calibration factors $\Delta\theta$ (in UI) and r (using the principal arctangent function) are computed from these intermediate parameters as follows:

Equation LI

$$\Delta\theta = \left(\frac{1}{2\pi}\right) Arc\tan[(X_U Y_V - X_V Y_U)/(X_U X_V + Y_V Y_U)]$$

Equation LII

$$r = [V/U] = \sqrt{\frac{X_V^2 + Y_V^2}{X_U^2 + Y_U^2}}$$

Low frequencies: inside ±300 kHz (i.e. *Freq* inside ±0.00375)

At low frequencies, no new quadrature calibration factors r and $\Delta\theta$ are generated. Instead, the factors last produced are used to improve accuracy. The factor $\Delta\theta$ is added to the phase value ϕ by adder 260. The sum (fractional part) is used to address cosine table U 228 and sine table U 232. The results of these tables provide input to ALUs $\mathbf{D}\cdot\mathbf{C}_U$ 204i, $\mathbf{E}\cdot\mathbf{C}_U$ 204j and $\mathbf{D}\cdot\mathbf{S}_U$ 204k, $\mathbf{E}\cdot\mathbf{S}_U$ 204l, respectively, as shown in Figure 4. Previously generated parameter r is used, in conjunction with all 12 dot products, to produce two intermediate parameters X_V and Y_V as follows:

Equation LIII

$$X_V = (\mathbf{E}\cdot\mathbf{S} + \mathbf{D}\cdot\mathbf{C}_U)(\mathbf{D}\cdot\mathbf{V} + r\mathbf{E}\cdot\mathbf{U}) + (\mathbf{E}\cdot\mathbf{C}_U - \mathbf{D}\cdot\mathbf{S})(\mathbf{E}\cdot\mathbf{V} - r\mathbf{D}\cdot\mathbf{U})$$

Equation LIV

$$Y_V = (\mathbf{D}\cdot\mathbf{S}_U - \mathbf{E}\cdot\mathbf{C})(\mathbf{D}\cdot\mathbf{V} + r\mathbf{E}\cdot\mathbf{U}) + (\mathbf{D}\cdot\mathbf{C} + \mathbf{E}\cdot\mathbf{S}_U)(\mathbf{E}\cdot\mathbf{V} - r\mathbf{D}\cdot\mathbf{U})$$

All frequencies: inside ±39.7 MHz (i.e. *Freq* inside ±0.49625)

Regardless of the computation of intermediate parameters X_V and Y_V in either the normal or low frequency mode, the phase correction computerized parameter θ_{cor} is computed using the four-quadrant arctangent function as follows:

Equation LV

$$\theta_{cor} = \left(\frac{1}{2\pi}\right) \arctan(X_V, Y_V)$$

In either normal or low frequency mode, the magnitude estimate of inphase signal *V* 148 is formally given by:

Equation LVI

$$V = \sqrt{X_V^2 + Y_V^2} \,/\, \det$$

However, the computation for X_V and Y_V, is signal frequency dependent as previously described. The computation of the determinant is also signal frequency dependent.

For normal frequencies, the determinant is:

Equation LVII

$$\det = (\mathbf{E}\cdot\mathbf{S})(\mathbf{D}\cdot\mathbf{C}) - (\mathbf{D}\cdot\mathbf{S})(\mathbf{E}\cdot\mathbf{C})$$

For low frequencies, the determinant is:

Equation LVIII

$$\det = (\mathbf{D}\cdot\mathbf{C} + \mathbf{E}\cdot\mathbf{S}_U)(\mathbf{E}\cdot\mathbf{S} + \mathbf{D}\cdot\mathbf{C}_U) + (\mathbf{E}\cdot\mathbf{C}_U - \mathbf{D}\cdot\mathbf{S})(\mathbf{E}\cdot\mathbf{C} - \mathbf{D}\cdot\mathbf{S}_U)$$

In one form of the invention, digital processing block 210 is implemented as a field programmable gate array (FPGA). In an alternative embodiment, digital processing block 210 is implemented as a DSP processor.

In one embodiment, as soon as computation of θ_{cor} and *Freq* values is completed by digital processing block 210, the increment value of phase accumulator 208 is modified by digital processing block 210 to $Freq - \theta_{cor}$ for one clock cycle, then to *Freq* for the next 255 clock cycles. The value of *Freq*, which is no larger than 1/2, should be carried to a precision of 17 bits.

The above process is then repeated for the next 256-sample segment. Throughout the process, the clocked phase accumulator 208 output $\phi(t_i)$ serves as a good digitized representation of the phase progression of the incoming inphase signal 148 to 25 bits of whole numbers and 10 bits of fractional numbers.

The embodiments of the invention described herein, including generating a quadrature signal and phase digitizing the quadrature signal, provide a heterodyne interferometer without a low frequency limitation. The quadrature

signal allows the frequency to be positive, zero, or negative without hindering phase digitizing. At normal frequencies, the inphase signal is used to determine the phase progression and parameters representing the imperfections of the quadrature signal are measured and exported. At low frequencies, both the inphase and quadrature signals waveform samples and the exported parameters are used to determine the phase progression.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.